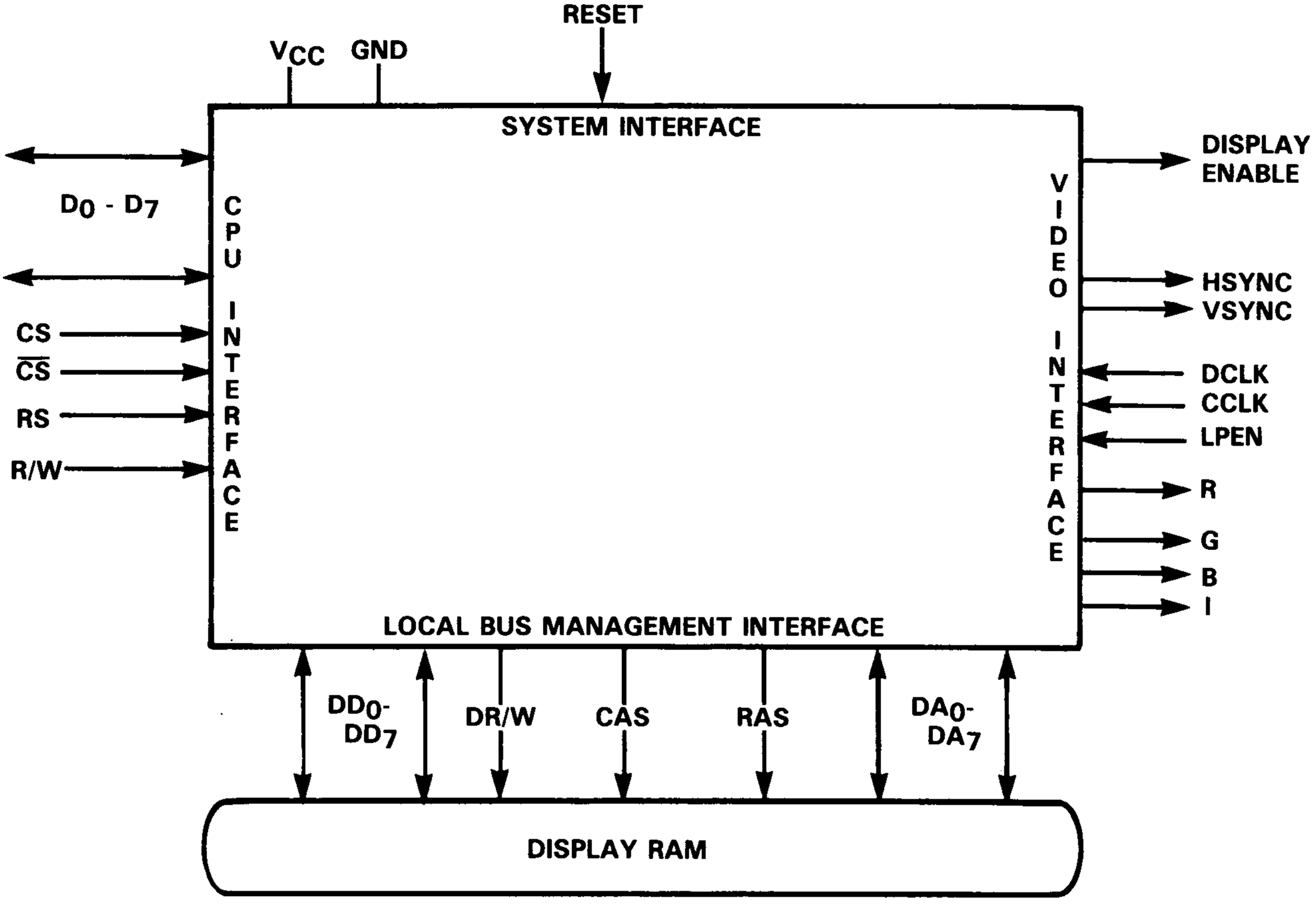
THE 8563 VIDEO CONTROLLER

FOLD OUT SCHEMATIC SHEET 3, PAGE 75, FOR EASY REFERENCE.

The 8563 is a HMOSII technology, custom, 80 column, color video display controller. The 8563 supplies all necessary signals to directly interface to 16K of DRAM, including refresh, and generates RGBI for use with an external RGBI monitor.



There are many different signals involved with the 8563 chip, but they can generally be divided into three categories. The CPU Interface signals serve as an interface to the 8502 bus. The Local Bus Management signals serve to maintain the local memory bus. Finally, the Video Interface signals are those signals that are necessary to provide an RGBI image on an RGBI monitor.

The 8563 chip interfaces directly to the 8502 bus using a minimum of signals. This is due mainly to the local memory used by the 8563.

The Local Bus Management Interface is a group of signals generated by the 8563 for the management of local video DRAM. This local DRAM both simplifies the addition of an 80 column video display to the system and enables it to support an 80 column display without taxing its memory resources.

The final set of 8563 signals are the Video Interface signals. These signals are directly related to the displayed video image.

External Registers

The 8563, which sits at $D600 in the C128, appears to the user as a device consisting of only two registers. These two registers are indirect registers which must be programmed to access the internal set of thirty-seven programming registers. The first register, located at $D600, is called the Address/Status register. When written to, the five least significant bits convey the address of an internal register to be accessed in some way. On a read of this register, a status byte is returned. Bit 7 of this register is low while display memory is being updated, and goes high when ready for the next operation. The 6th bit will return low for a light pen register invalid condition and high for a valid light pen address. The final register indicates with a low that the scan is not in vertical blanking, high that it is in vertical blanking.

The other register is the data register. It can be read and written to. Its purpose is to write data to the internal register selected by the Address register. All internal registers can be read and written to through this register, though not all of them are a full eight bits wide.

Internal Registers

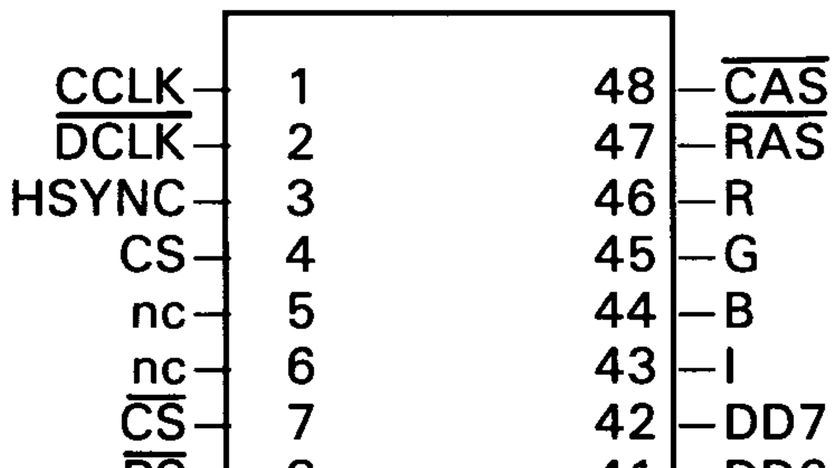
There are thirty-seven internal registers in the 8563, used for a variety of operations. They fall into two basic groups — setup registers and display registers. Setup registers are used to define internal counts for proper video display.

The display registers are used to define and manipulate characters on the screen. Once a character set has been downloaded to the chip, it is possible to display 80 column text in 4-bit digital color. There are also block movement commands that remove the time overhead needed to load large amounts of data to the chip through the two levels of indirection. Below is a display of the 8563 internal register map.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R00	Horizontal Total							
R01	Horizontal Displayed							
R02	Horizontal Sync Position							
R03	Vertical Sync Width				Horizontal Sync Width			
R04	Vertical Total							
R05				Vertical Total Adjust				
R06	Vertical Displayed							
R07	Vertical Sync Position							
R08							Interlace Mode	
R09				Character Total Vertical				
R10		Cursor Mode		Cursor Start Scan Line				
R11				Cursor End Scan Line				
R12	Display Start Address (High)							
R13	Display Start Address (Low)							
R14	Cursor Position (High)							
R15	Cursor Position (Low)							
R16	Light Pen Vertical							
R17	Light Pen Horizontal							
R18	Update Location (High)							
R19	Update Location (Low)							
R20	Attribute Start Address (High)							
R21	Attribute Start Address (Low)							
R22	Character Total-Horizontal				Character Displayed-Horizontal			
R23				Character Displayed-Vertical				
R24	Copy/Fill	Rev Screen	Blink Rate	Vertical Smooth Scroll				
R25	Graph/Text	Attb Enb	Semigraph	Pix Dbl	Horizontal Smooth Scroll			
R26	Foreground Color				Background Color			
R27	Address Increment per Row							
R28	Character Set Address			4164/4416				
R29				Underline Scan Line				
R30	Word Count (count-1)							
R31	CPU Read/Write Data							
R32	Block Copy Source Address (High)							
R33	Block Copy Source Address (Low)							
R34	Display Enable Begin							
R35	Display Enable End							
R36					DRAM Refresh per Scan Line			

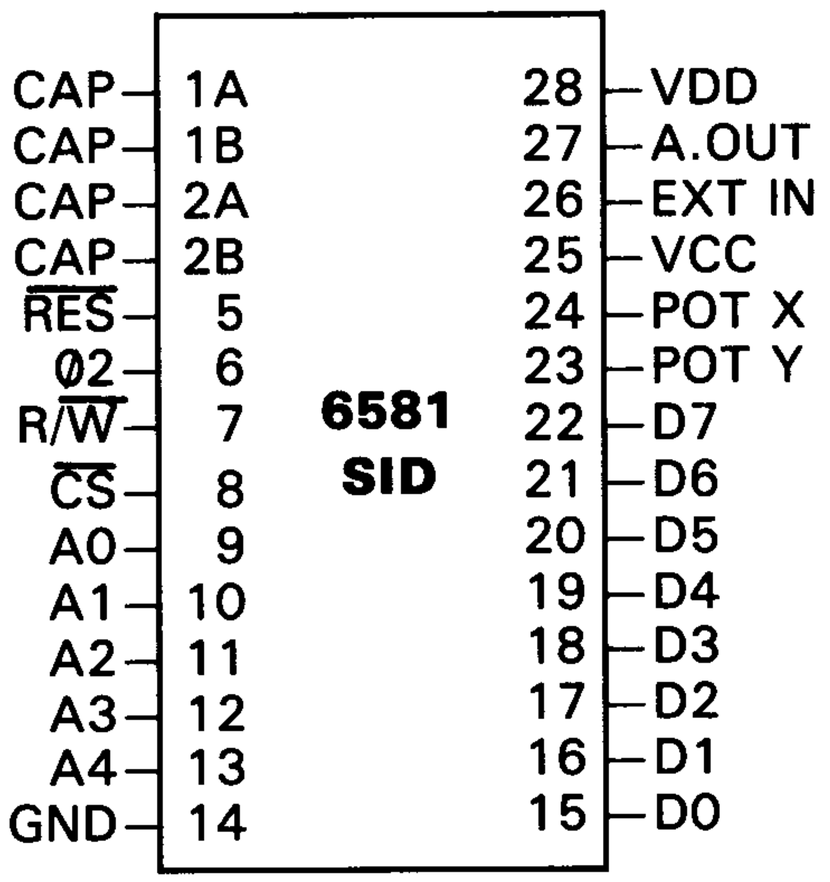
8563 REGISTER MAP

315014
8563 CRT VIDEO CONTROLLER



1	CCLK	Character Clock output.
2	DCLK	Video Dot Clock D.
3	HSYNC	Horizontal Sync Signal.
4	CS	Chip Select input, active high.
5,6	NC	No Connection.
7	CS	Chip Select input, active low.
8	RS	Register Select input. A high allows reads & writes to the selected data register. A low allows reads of the Status register and writes to the Address register.
9	R/W	The read/write line controls the data direction for the data bus. Read is active high, write is active low.
10,11, 13-18	D0-D7	Bi-directional data bus.
12	VSS	Ground.
19	DISPEN	Display Enable output.
20	VSYNC	Vertical Sync signal.
21	DR/W	Local Display DRAM Read/Write.
22	INIT	Active low input for clearing internal control latches.
23	RES	Reset input that initializes all internal scan counters, but not control registers.
24	TEST	Used for testing only — tied to ground.
25	LPEN	Input for Light Pen. A positive going transition on this input latches the vertical and horizontal position of the character being displayed at that time.
26-33,	DA_0-DA_7	Local display DRAM address bus.
34-36, 38-42	DD_0-DD_7	Bidirectional local display DRAM data bus.
37	VCC	5VDC input.
43-46	R,G,B,I	Pixel Data Outputs. A four-bit code is formed, associated with each pixel, containing color/intensity information, allowing a total of 16 colors on grey shades to be displayed.
47	RAS	Row Address Strode for local DRAM.
48	CAS	Column Address Strobe for local DRAM.

906112
6581 SOUND INTERFACE DEVICE (SID)



1,2, 3,4	CAP1A,1B 2A,2B	Capacitor filter connections.
5	RES	Reset input. A low pulse initializes the SID.
6	Ø2	Processor phase 2 clock input.
7	R/W	Processor read/write input.
8	CS	Chip select input.
9-13	A0-A4	Address lines from processor.
14	GND	Dc ground connection.
15-22	D0-D7	Data Bus connections.
23	POT Y	Input to a A/D converter used to detect the value of a variable resistor. Commonly connected to game paddles.
24	POT X	Same as POT Y.
25	VCC	5VDC input.
26	EXT IN	External audio input.
27	Audio out	Audio output, AC coupled to audio amp.
28	VDD	12VDC input.

PIN DESCRIPTION

CPU INTERFACE

D0-D7	Bidirectional Data Bus interface to the CPU.
CS	Chip Select input (active high).
CS*	Chip Select input (active low).
RS	Register select input. A high allows reads and writes of the selected data register. A low allows reads of the Status Register and writes of the Address Register.
R/W	Read/write input to control D0-D7 data direction. A high allows the CPU to read data supplied by the CRT Controller. A low allows the CRT Controller to accept data written by the CPU.
INTR	Interrupt request output. An open-drain output that is driven low when the Update Ready status bit makes a 'zero' to 'one' transition. This output goes high-impedance when either the Update Ready status bit is a 'zero' or the CPU reads the status register.

VIDEO INTERFACE

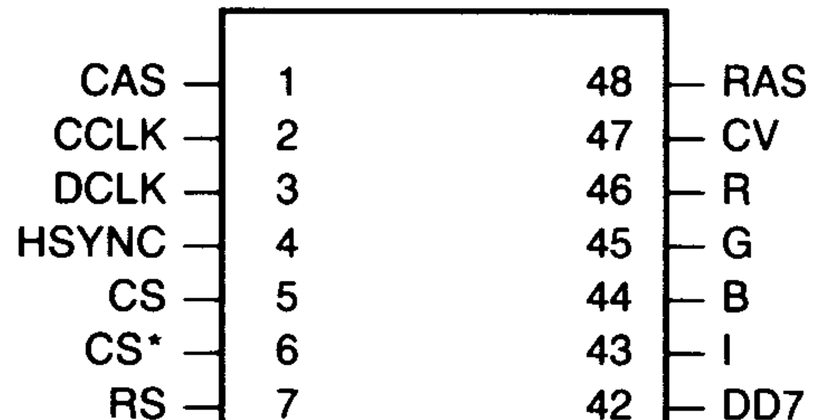
Vcc	5 VDC +/−5%
Vss	0 VDC
RES	Reset input to initalize all internal scan counter circuits. The control registers are not affected. RES can be used to synchronize the display frame to an externally generated signal. This signal should not be confused with the INIT input.
LPEN	Light pen input. A low-to-high transition of the LPEN input loads the internal light pen registers with the vertical and horizontal character poisitions.
DCLK	Dot clock input. Determines the pixel width, DCLK is divided internally to generate the internal character clock and DRAM signals.
HSYNC	Horizontal sync output. HSYNC polarity, position and duration are fully programmable.
VSYNC	Vertical sync output. VSYNC polarity, position and duration are fully programmable.
CSYNC	Composite SYNC output. This is the logical exculsive-nor of internal active-high HSYNC and VSYNC signals.
R, G, B, I	Red, Green, Blue and Intensity outputs. These output a four-bit code associated with each pixel. A total of 16 colors (or shades of gray) may be displayed.
CV	Composite Video output. This is the logical OR of the R, G, and B outputs.
DR/W	Video Display RAM read/write output signal.
DD0-DD7	Video Display RAM bidirectional Data Bus.
DA0-DA7	Video Display RAM multiplexed Address Bus outputs.
RAS	Row Address Strobe output for the multiplexed addresses.
CAS	Column address strobe output for the muliplexed addresses.
CCLK	Character clock output (for unspecified uses).
INIT	Initialization input pin (active low). Clears internal control latches, allowing the CRT Controller to begin proger operation following power-on initialization. The INIT pin should be held low for at least 16 DCLK cycles during system initialization, and held high during operation.
TEST	This pin reconfigures the part to simplify automatic testing. In normal use this pin should be connected to Vss.

IC 8568
80 COLUMN CRT CONTROLLER
PN #315092-01

This Circuit implements the features of the 6545E CRT Controller with additional features to increase system integration.

Features

- Single +5 volt power supply.
- Interlaced or non-interlaced display.
- NTSC or PAL operation.
- Shared RAM for Character Data, Pointers and Attributes.
- Cursor and Attributes decoded on-chip.
- R, G, B, I pixel outputs.
- Separate programmable Horizontal and Vertical Sync outputs.
- Character Clock generated on-chip.
- Interfaces to DRAMs with on-chip RAS/CAS timing.
- Programmable character fonts.
- Programmable frame height, width and rate.
- Directly interfaces to 4164 or 4416 DRAMs.



The device is a highly integrated text display chip designed to reduce the parts count of an 80-column display system. The CRT Controller contains the high-speed pixel frequency logic, requiring only a buffer to drive low impedance loads. The CRT Controller is capable of addressing 64K of DRAM memory for Character Data (character fonts), Character Pointers and Attributes. In addition, the DRAM signals RAS, CAS, Read/Write, Data and Multiplexed Addresses are generated on-chip and require no external logic to interface to the DRAMs. The DRAM multiplexed Addresses can be configured via a programmable register bit to interface directly to either 4164 or 4416 Type DRAMs

The device contains an internal 80-column double line buffer. This buffer is loaded with Character Pointers and Attributes during the Horizontal-Blanking interval (and any blank scan lines). These Pointers and Attributes are loaded during one displayed character row for use in the next character row. This device is equivalent to a 2568 or 8568.

The -01 version of the part is intended for use in systems with a TTL level Dclk signal. The -02 version is for systems with a CMOS level Dclk.

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Device:      DVDC
Part No:     8563
         8568

Display Format:  programmable up to up to 80x25 text, 640Hx400V bitmap
         (interlaced up to 80x50 text, 640Hx480V bitmap, and more)
Display Modes:   3 char modes: Std, Semigraph and pixel,
         double width & HiRes bitmap mode
Video Output:    digital RGBI 16 color or 16 gray-shades
Features: 8563:  interlace/non-interlace, horiz & vert scroll,
         lightpen input, hardware cursor, underline, blink and
         reverse video, supports 2 character sets of 256 each
       8568:  above plus Update Ready Interrupt, composite video and
         composite sync
Memory Interface:access 64K, programmable to interface either 4164/4464 or
         4416 DRAM
Pins:        48
Supply:      +5V


     Make sure you get one that says R9a or R9b after the 8568.
     These are later Revisions that seem to work better.

Pinout

Pin 8563

 1  CCLK
 2  DCLK
 3  HSYN
 4  /CS
 5  -
 6  -
 7  /CS
 8  /RS
 9  R/W
10  D7
11  D6
12  Vss
13  D5
14  D4
15  D3
16  D2
17  D1
18  D0
19  DISPEN
20  VSYN
21  DR/W
22  INIT
23  /RES
24  TST

25  /LP2
26  DA0
27  DA1
28  DA2
29  DA3
30  DA4
31  DA5
32  DA6
33  DA7
34  DD0
35  DD1
36  DD2
37  Vdd
38  DD3
39  DD4
40  DD5
41  DD6
42  DD7
43  I
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44 B
45 G
46 R
47 /RAS
48 /CAS

The VDC VideoRAM Upgrade

From: Raymond Carlsen <rrcc@u.washington.edu>
Newsgroups: comp.sys.cbm
Subject: Re: W: 8563 RAM swap instructions
Date: Wed, 27 Sep 1995 20:50:02 -0700

> The subject says it all. How do you do this 16k to 64k swap?

I assume you mean the video RAM upgrade for the C-128. If you're good with a de-soldering iron, it just involves removing two chips from the board and installing replacements. The original chips are 4416 DRAM at board locations U23 and U25 inside the metal can, between the VIC and RGB chips. The replacements are 4464. The numbers on the chips may vary with manufacturers, but the originals are 4 bit wide 16K... two of them make 16K by 8 bits. The upgrade to two 4 bit wide 64K chips give a total of 64K by 8 for the flat 128. The 128D was built with 64K of VRAM already installed.

I always install sockets anytime I replace chips in a PC board. Removing the old chips is the worst part of the job. Probably the easiest way is to cut all of the pins on the old chip, then remove them one at a time with a regular iron. As a tech, I hate to destroy anything that still works. I use a desoldering iron to free each pin, then remove the chip intact. If the new chips don't work for any reason, I can cross check my work by reinstalling the old ones. Sockets mean never having to solder again. It's important to orient the new chips in the board correctly. One end of the chip will have a notch and the outline on the board will match.

Unless you have software that takes advantage of the extra video RAM you will not see any difference in the performance of your computer. I think Maverick uses that RAM space to speed up copying files. It's useful for improved bitmapped graphics. It is only good for the 80 column screen... the 40 column VIC doesn't access it. To verify C-128 VRAM as either 16K or 64K, run this little program:

```
POKE DEC("D600"),28:POKE DEC("D601"),63:SYS DEC("FF62"):SCNCLR  <RETURN>
```

If the screen shows the READY prompt and looks normal, the 128 has 64K of VRAM installed. If it only has 16K (stock 128 without upgrade), the screen fills up with zeros. Hit RUN/STOP-RESTORE to clear it.

At one time, some company was selling a piggyback board with the RAM installed. It needed no soldering as the on-board 4116s were bypassed. All that was necessary was to remove the 80 Column RGB (8563, also known as the VDC) chip from its' socket, install the piggyback board and plug the RGB chip into the piggyback. I haven't seen that board advertised for some time.

[Chips are available from Jameco Electronics @ 1-800-831-4242. Order part #41582 (41464-12), or 41574 (41464-10), or 41611 (41464-80). They cost less than 3 bucks each. Jameco also has other replacement chips for Commodore computers.]

Ray Carlsen Univ. of Washington, Seattle

Uncovered: The VDC 8568's 38th register

Ok you,re probably already thinking, "but the VDC has only 37 registers, hasn't it?"
This is quite correct for the old 8563 types inside the C128 and C128D.
Inside the C128DCR, however, a later version with different new characteristics had been installed.
One of them is an additional register!

by Nicolas Welte

The existance of register 37 (you start counting at 0) had already been reported about by 64'er magazine,
but there hasn't even been a hint of an explanation of the register's function.
This should finally be made up for with this article.
Only bits 7 and 6 are available, all other bits are 'reserved' and will always read back as 1.
Following a hardware reset, though, bits 7 and 6 are also 1,
so that reading the register will return 255 just as with all other unused registers.
Only when writing into the register, the difference will become apparent,
and in a really big way to boot: the screen loses synchronization and the picture runs through.
This is not a useful effect, of course.
Some measuring at video output returned the following function: bit 7 controls the horizontal sync signal's polarity.
That signal is found at the RGBI connector. In the same way, the vertical sync signal at pin 9 is controlled by bit 6.
In this case, polarity refers to whether the synchronisation pulse is directed from TTL 0 to 1 (positive) or from 1 to 0 (negative).
By default, the C128 works with positive pulses for both signals, and all monitors are designed for that.
This leads to following register map, which you should glue into the manual:
[table is printed in the issue]
Is there any advantage we can get from this register? Yes, indeed there is!
But in order to gain it, you need an EGA monitor.
EGA monitors were the first high resolution monitors for PCs that really deserved the name.
These monitors work with two different fixed frequency modes, one of which is comaptible with older CGA cards,
and therefore with the C128's RGBI output.
The other mode works at a line frequency of about 21kHz and a resolution of 640x350 at a vertical refresh rate of 60Hz, though.
EGA also offers 64 colors instead of just 16 colors, but of course this feature can't be used by a C128.
Some C128 owners may be using such a monitor, as they offer a better display quality than older CGA models.
These days, they can be bought for a song as well.
How does the EGA monitor know in which of its two modes it should work? One option would be an automatic detection of the line frequency,
but the time hadn't come for that technology yet.
Thus, the monitor needed a signal from the outside indicating which mode should be chosen.
This is realized by the sync signals' polarity!
Four different modes could therefore be chosen, but my monitor in particular knows only two.
There are also modern multi frequency monitors which ignore this signaling and switch automatically.
There are two example programs on the cover disk, which will only run on a C128DCR.
Those of you who are sure you have a monitor which switches automatically, may remove line 5 from the program, which will allow the programs to run on old C128s and C128Ds.
In all cases, you should be absolutely sure that a monitor is connected which can handle 21kHz, otherwise, there can be significant damage!
Two different versions are given, a 50Hz version and a 60Hz version, sensibly named EGA50HZ and EGA60HZ.
The 60Hz version displays a text screen with 77 columns and 43 lines roughly resembling PC's EGA standard.
At least for me, the 50Hz version works better, perhaps due to the fact that I have a 50Hz mains current as well.
This allows for 77 columns and 52 lines, without any interlace flickering!
Unfortunately, 77 columns are the absolute maximum with attributes turned off.

[Read more about this topic in the current GO64!-issue]