THE PROGRAMMED LOGIC ARRAY

FOLD OUT SCHEMATIC SHEET 2, PAGE 74, FOR EASY REFERENCE.

The 8721 C128 PLA is a programmed version of the Commodore 48 Pin Programmable Logic Array. It provides all of the chip selects and other decoded signals that were necessary for the C64, along with a number of such signals new in the C128 system.

Summary of PLA functions:

- Control all ROM selects (KERNAL, BASIC, FUNCTION, EXTERNAL) in all operating modes.
- VIC chip select.
- Color RAM chip select.
- Character RAM chip select.
- Gated write enable to color RAM.
- Latched write enable to DRAMs.
- Z-80 select decoding.
- Z-80, I/O decoding, for Z-80 I/O cycle and Z-80 memory mapping.
- Data bus direction signal.
- I/O group chip select (includes I/O-1, I/O-2, CIA-1, CIA-2, SID, 8563).
- I/O access signal indicating an I/O operation is occuring.
- Column Address Strobe Enable for DRAM.

Chip Select Generation

The PLA device is responsible for defining the banking rules for ROM and RAM that the system will follow. The chip generates chip selects for all ROM and the VIC chip. It generates an enable for any other I/O device in the map, and can enable or disable CAS based upon what else is enabled. In C128 mode, decisions are made using the processor addresses and the four mode status lines: ROMBANKLO, ROMBANKHI, I/O SELECT, and C128/64. The C128 mode banking scheme is quite straightforward and simple. In Z-80 mode, the selection mechanism becomes even simpler, thanks to the I/O cycle of the Z-80 processor.

C64 chip selects account for the bulk of the PLA font. The C64 selects I/O, RAM, and ROM based upon the internal control lines BA, HIRAM, LORAM, and CHAREN. The status of these lines, and the decoded addresses, determine for any given time which, if any, chip is selected. When a cartridge is inserted, two additional control lines come into play — $\overline{\text{EXROM}}$ and $\overline{\text{GAME}}$. Various combinations of these lines cause different memory maps to be asserted, all based upon the PLA font.

Other PLA Functions

The PLA performs a variety of functions other than chip selects. It creates the write enable strobes for both DRAM and Color RAM. In C128 mode, the C64 control lines HIRAM, LORAM, and CHAREN are not needed, since the MMU controls the more sophisticated C128 method of banking. Thus, these lines are used to extend the functionality of the C128 at little or no additional cost in hardware. The CHAREN line is used in C128 mode to turn the Character ROM on and off in VIC address space. In the C64, the presence of this ROM was a function of the VIC bank selected. In C128 mode, the ROM can appear or disappear in any VIC bank.

The second of the new functions uses LORAM and HIRAM to select one of two Color RAM banks. The level of LORAM selects the bank that will be seen during processor time, the level of HIRAM selects the bank that will be seen during VIC time. Thus, a program can swap between two full color pictures very clearly, or the processor can modify one full color picture while displaying another.

PROGRAMMED LOGIC ARRAY (Continued)

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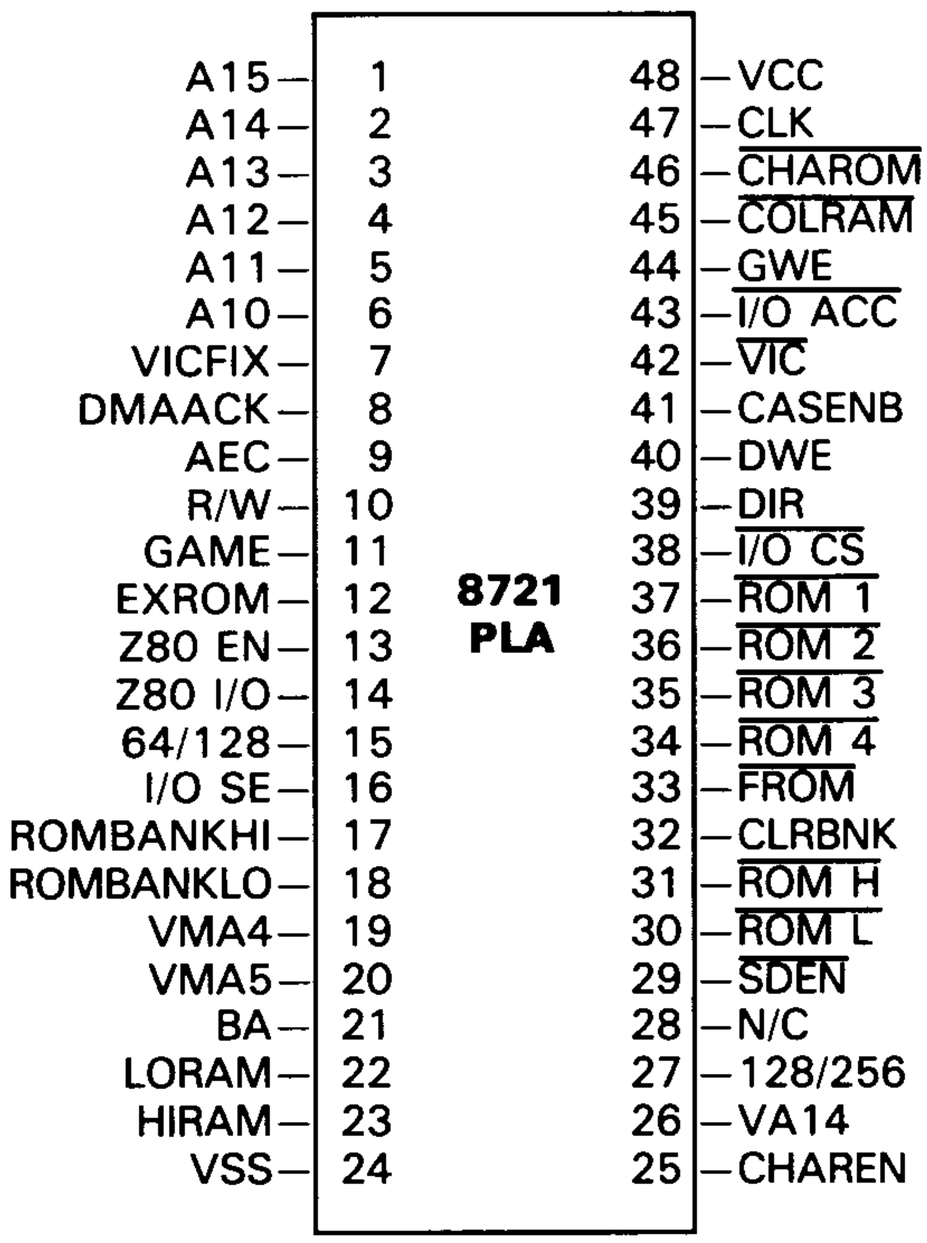
PROGRAMMABLE LOGIC ARRAY



1-6	A_{10}-A_{15}	Address input from 8502 microprocessor.
7	VICFIX	Input to modify CASENB latching for VIC timing.
8	DMAACK	DMA Acknowledge input pulled high in C128 system.
9	AEC	Address Enable Control input from VIC.
10	R/W	Read/Write input from 8502 microprocessor.
11	GAME	Input from the expansion port indicating an external ROM in C64 mode. Unused in C128 mode.
12	EXROM	Input from the expansion port indicating an external ROM in C64 mode. Unused in C128 mode.
13	Z80EN	Input from the Z80 BUSACK line indicating the Z-80 relinquishes the bus.
14	Z80 I/O	Z80 input requesting I/O.
15	64/128	High input sets C128 mode.
16	I/O SE	I/O select input from MMU.
17,18	ROMBANKLO ROMBANKHI	Input from MMU to indicate ROM bank status.
19,20	VMA_4,VMA_5	Input from VIC multiplexed address.
21	BA	Bus Available Input from VIC.
22, 23, 25	LORAM HIRAM CHAREN	Memory configuration signals input from the 8502 port. They are used for C64 mode memory mapping and C128 mode extensions.
24	VSS	Ground
26	VA14	VIC address 14 input from the 6526. Selects video map in C64 mode.
27	128/256	Input line to indicate whether 128K or 256K ROMs are installed in the system. High for 128K, low for 256K.
28	N/C	No connection.
29	SDEN	SD enable output used to enable the buffer between the data bus and the S DATA bus.
30,31	ROM L, ROM H	Active low outputs. They are the chip selects for expansion ROMs.
32	CLRBNK	Output for color RAM bank select.
33	FROM	Function ROM chip select output. Active low.
34-37	ROM 1-4	ROM chip selects for operating system ROM. Active low output.
38	I/O CAS	Active low output used as I/O chip select. Enables external decoder for CIA1 and 2, I/O 1 and SID and 8563.
39	DIR	Data Bus Direction control output for the Data to S Data buffer.
40	DWE	Active low output for DRAM write enable. MUX latches the output in the PLA.
41	CASENB	RAM Column Address Strobe Enable. Used to gate CAS outputs from MMU. The active low output is latched by MUX in the PLA.
42	VIC	Active low output to select the VIC chip.
43	I/O ACC	Indicates access to a 1 MHz part, typically an I/O part. Used by the VIC to stretch the 2 MHz clock.
44	GWE	Active low output used as write enable for color RAM.
45	COLRAM	Color RAM chip select, valid for MPU and VIC.
46	CHAROM	Character ROM chip select, valid for MPU and VIC.
47	CLK	Common clock input from VIC.
48	VCC	5VDC input.