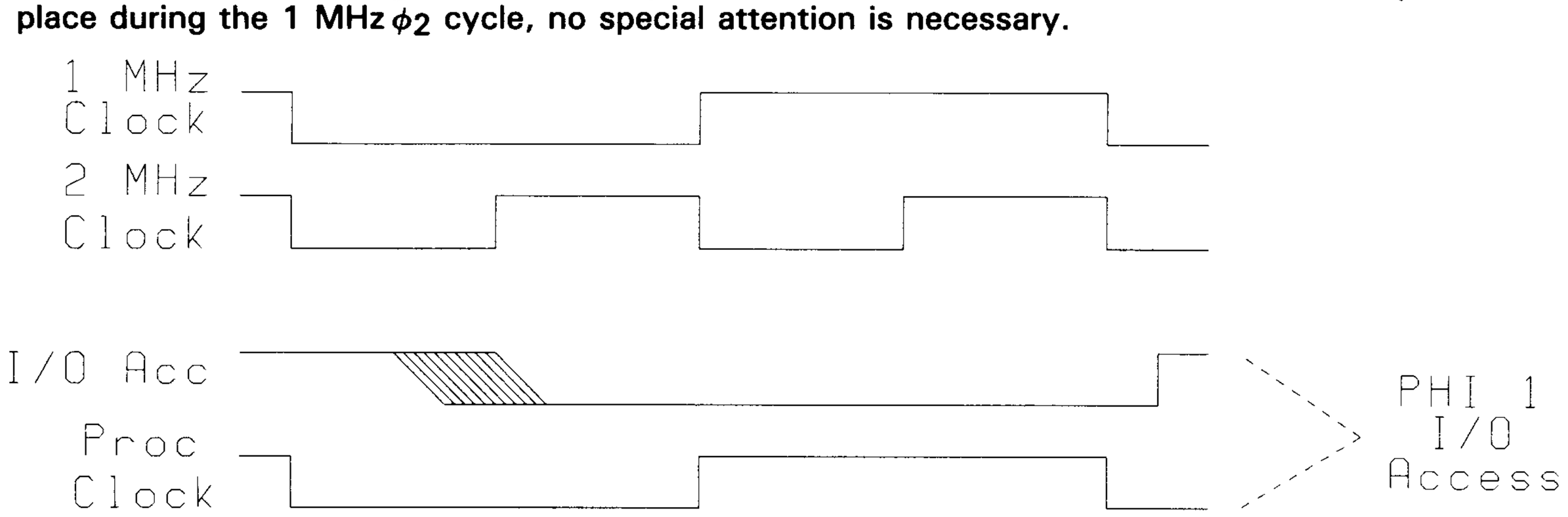
THE 8502 MICROPROCESSOR

FOLD OUT SCHEMATIC SHEET 2, PAGE 74, FOR EASY REFERENCE.

The 8502 is an HMOSII Technology microprocessor similar to the 6510/6502. It is the normal operating processor and is used in the C64 and the C128 modes. Fully software compatible with the 6510, hence the 6502, the 8502 also features a zero page port used in memory management and cassette implementations. The 8502 is also specified for operation at 2 MHz. The 2 MHz operation is made possible by removing the VIC from the system. The VIC chip is never completely removed from the C128 system, as it continues to function as clock generator and bus arbitrator. However, the VIC is removed as a display chip and co-processor, thus the full clock cycle can be devoted to processor functioning instead of sharing the cycle with the VIC. The task of video display processor is then taken over by the 8563, which can function without the need for bus sharing that the VIC required. Since the I/O devices, SID, etc., are rated at 1 MHz only, stretching of the 2 MHz clock is used to allow these parts to be directly accessed by the 2 MHz processor, and still keep throughput to a maximum. The I/O devices are not affected by the 2 MHz operation as they are still driven by a 1 MHz source (and as such, all timer operations remain unchanged), and clock stretching is only used to synchronize the 2 MHz machine cycle to the 1 MHz ϕ_0 high time. The clock sources and clock stretching capabilities are generated by the VIC chip.

CLOCK STRETCHING

When running in 2 MHz mode, the processor clock sometimes must be stretched. This is handled by the VIC chip, the processor, and the PLA working together. When an I/O operation is decoded during a 2 MHz cycle, the phase relationship between the 2 MHz and the 1 MHz clocks must be considered. If the 2 MHz access occurs during 1 MHz ϕ_1, the access to a clocked I/O chip would be out of synchronization with the 1 MHz clock that drives all I/O chips. Thus, during this phase relationship, $\overline{\text{IOACC}}$, from the PLA, signals the VIC chip to extend the 2 MHz clock. Should the 2 MHz cycles take place during the 1 MHz ϕ_2 cycle, no special attention is necessary.



Clock Stretching in 2 MHz Mode

Please take note to consider the speed implications of this. In 2 MHz mode, half of the I/O accesses given will occur at an effective speed of 1 MHz. For time critical operations, then, accesses to I/O chips are kept at a minimum.

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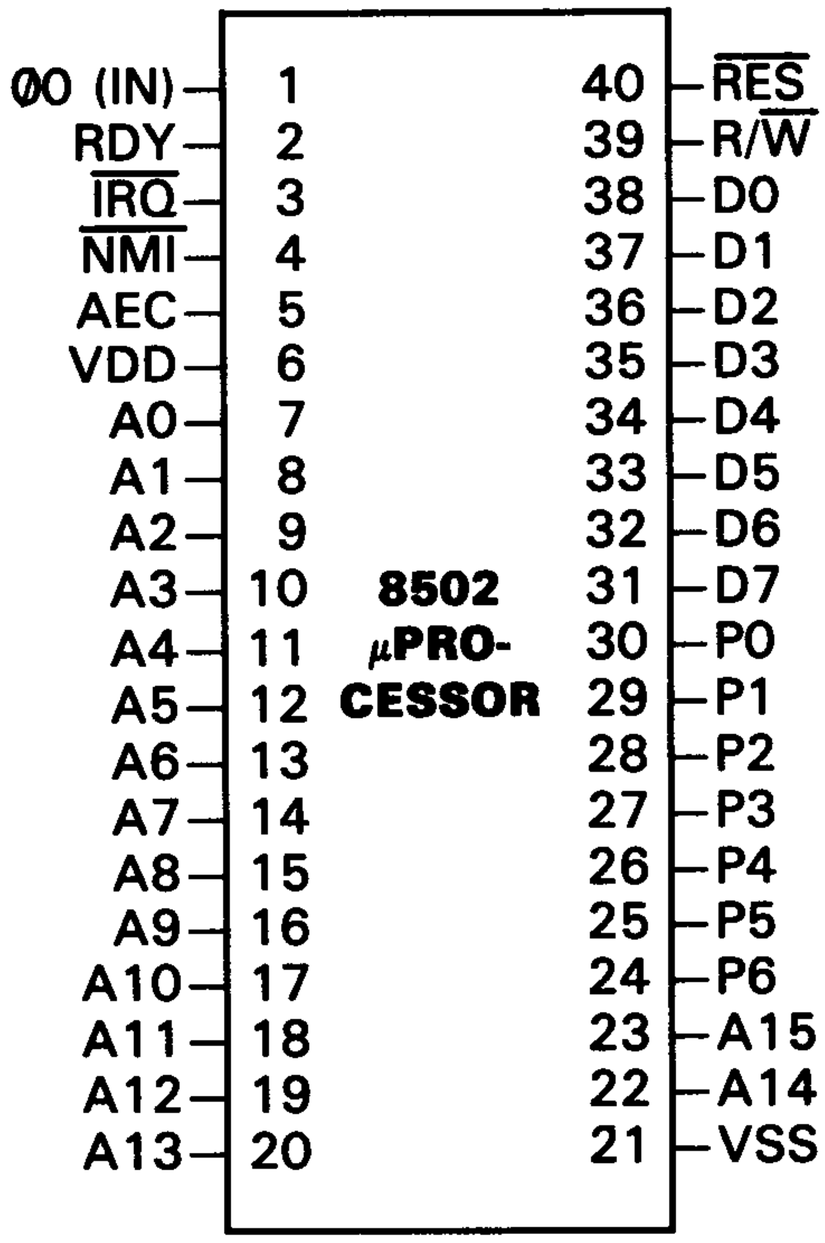

1	Ø0	Phase 0 clock input. This is the dual speed system clock for the 128.
2	RDY	Ready. TTL level input, used to DMA the 8502. The processor operates normally while RDY is high. When RDY makes a transition to the low state, the processor will finish the operation it is on, and any subsequent operation if it is a write cycle. On the next occurrence of read cycle the processor will halt, making it possible to tri-state the processor to gain complete access to the system bus.
3	IRQ	The Interrupt Request input is a request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request. At that time, the interrupt mask in the Status Code Register will be examined. If the interrupt mask is not set, the processor will begin an interrupt sequence. The Program Counter and the Processor status register will be stored on the stack and the interrupt disable flag is set so that no other interrupts can occur. The processor will then load the program counter from the memory location $FFFE and $FFFF.
4	NMI	The Non-Maskable Interrupt Request is a negative-edge sensitive request that the processor initiate an interrupt sequence. The processor will complete execution of the current instruction before recognizing the request. The Program Counter and the processor status register will be stored on the stack. The processor will then load the program counter from the memory locations $FFFA and $FFFB.
5	AEC	The Address Enable Control. The Address Bus is only valid when the AEC line is high. When low, the address bus is in a high impedance state. This allows DMA's for dual processor systems.
6	VDD	5VDC input.
7-20 22,23	A0-A15	Address bus outputs. Unidirectional bus used to address memory and I/O devices. The address bus can be disabled by controlling the AEC input.
21	VSS	DC ground.
24-30	P0-P6	Bidirectional I/O port used for transferring data to and from the processor directly. The Data Register is located at location $0001 and the Data Direction Register is located at location $0000.
31-38	D0-D7	Bi-directional bus for transferring data to and from the device and the peripherals.
39	R/W	The read/write line is a TTL level output from the processor to control the direction of data transfer between the processor and memory, peripherals, etc. This line is high for reading memory and low for writing.
40	RES	The Reset input is used to reset or start the µprocessor from a power down condition. During the time that this line is held low, writing to or from the µprocessor is inhibited. When a positive edge is detected on the input, the µprocessor will immediately begin the reset sequence. After a system initialization time of 6 cycles, the mask interrupt flag will be set and the processor will load the program counter from the contents of the memory locations $FFFC and $FFFD. This is the start location for program control. After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least 2 cycles. At this time the R/W line will become valid.