THE 8564 VIDEO INTERFACE CHIP

FOLD OUT SCHEMATIC SHEET 3, PAGE 75, FOR EASY REFERENCE.

The 8564 VIC chip used in the C128 is an updated version of the VIC chip used in current C64 systems. It contains all of the video capabilities of the earlier 6567 VIC chip, including high resolution bit mapped graphics and movable image blocks. It also supports new features used by the C128 system, including extended keyboard scanning. Its register map is upward compatible with the old VIC, allowing compatibility in C64 mode. It is powered by a single 5V DC source, instead of the two sources required by the old VIC chip.

Summary of functions that remain the same as the 6567 VIC:

- Standard Color Character Display Mode
- Multicolor Character Display Mode
- Extended Color Character Display Mode
- Standard Bit Map Mode
- Multicolor Bit Map Mode
- Movable Image Blocks
- Movable Image Block Magnification
- Movable Image Block Priority
- Movable Image Block Collision Detection
- Screen Blanking
- Row/Column Display Select
- Smooth Scrolling
- Light Pen
- Raster Compare Interrupt

As these functions exist in the previous VIC, their description is purposely kept to a minimum. The new functions, however, are described in detail below. Additional Functions of 8564 VIC:

Extended Keyboard Scanning

The 8564 contains a register called the **Keyboard Control Register.** This register allows scanning of three additional keyboard control lines on the C128 keyboard. Thus, the C128 keyboard can have advanced additional keys in C128 mode, while still retaining complete C64 keyboard compatibility in C64 mode. In this register, register 47, bits 0-2 are directly reflected in output lines K_0 to K_2, while bits 3-7 are unused, returning high when read.

2 MHz Operation

The VIC chip contains a register which allows the C128 system to operate at 2 MHz instead of the standard 1 MHz of the C64. This operating speed, however, disallows the use of the VIC chip as a display processor. This bit is bit zero in register 48, and setting this bit enables 2 MHz mode. During 2 MHz operation, the VIC is disabled as a video processor. The μProcessor spends the cycle full time on the bus, while VIC is responsible only for dynamic RAM refresh and DMA arbitration. Clearing this bit will bring back 1 MHz operation and allow the use of the VIC as a video display chip. During refresh and I/O access, the system clock is forced to 1 MHz regardless of the setting of this bit.

Bit one of this register contains a chip testing facility. For normal operation this bit must be clear. None of the other bits in this register are connected.

System Clock Control

The new VIC chip generates several clocks used by the C128 system. The main clock is the 1 MHz clock, which operates at approximately 1 MHz at all times. Most bus operations and all I/O operations take place in reference to this clock. The next clock to consider is the 2 MHz clock. This clock clocks selected system components, such as the processor, at 2 MHz when in 2 MHz mode. The VIC chip monitors the $\overline{\text{IOACC}}$ input, which indicates the access of an I/O chip, and when asserted, will stretch the 2 MHz clock to synchronize all 2 MHz parts with the 1 MHz I/O parts. Finally, the last clock is the Z-80 clock, which is a 4 MHz clock that only takes place during the low half of the 1 MHz clock. One final note is that since I/O parts look only at the 1 MHz clock, all I/O timings remain the same no matter what the 2 MHz clock is doing.

DMA and Bus Arbitration

True DMA of the internal processor can now be accomplished by requesting the DMA through VIC. The VIC will shut down the processor in an orderly fashion, instead of a suicidal fashion. A DMA source requests a DMA via the DMARQST input. VIC will respond to that request with a DMAACK after shutting down the processor. The DMA source must listen to the DMAACK line and be prepared to itself be shut down in the event that VIC decides to do its own DMA. Thus, the VIC chip has the highest DMA priority. The C128 system does not use this DMA arbitration scheme, but a fatal DMA scheme similar to that of the C64.

THE 8564 VIDEO INTERFACE CHIP (Continued)

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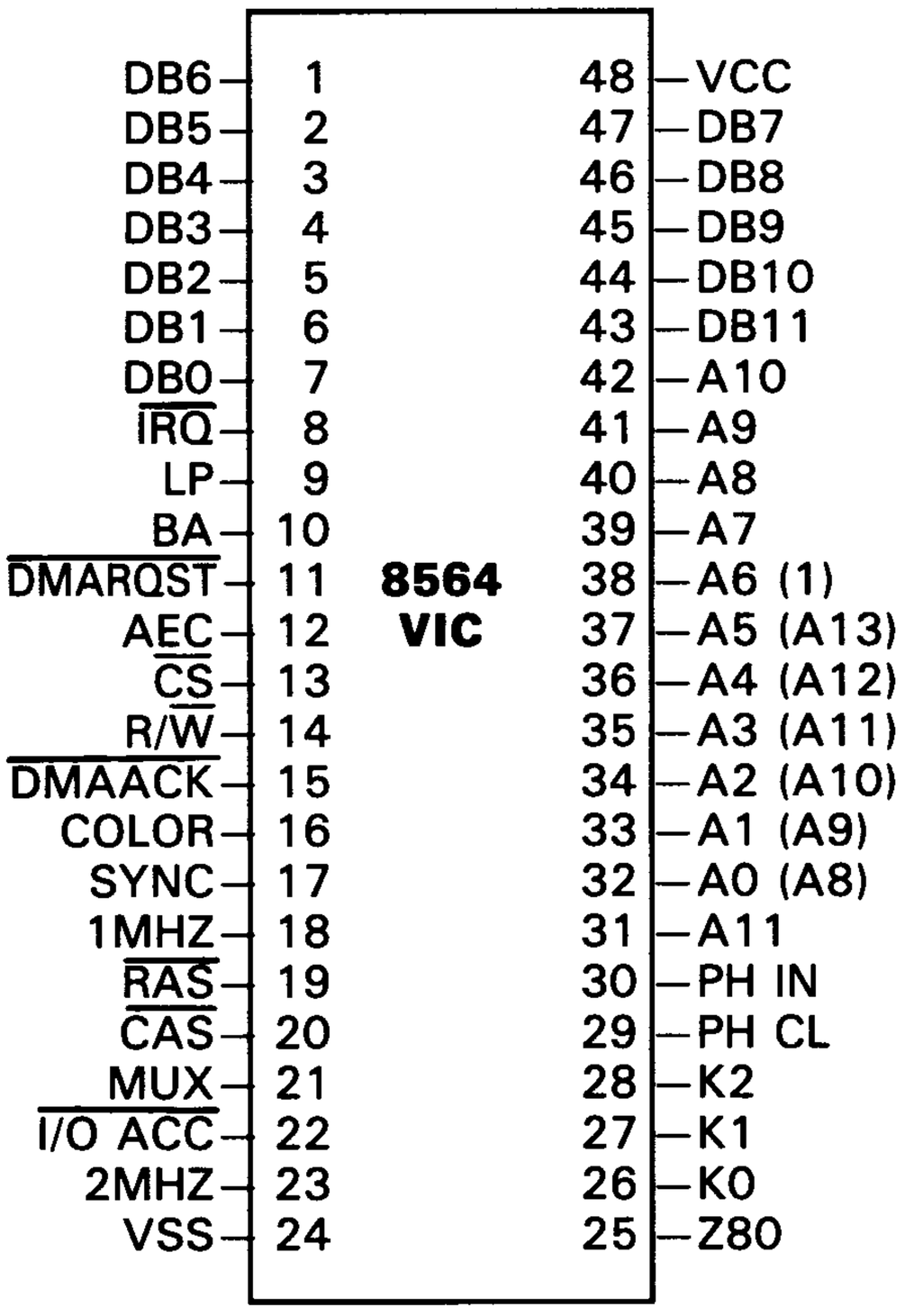
8564 VIDEO INTERFACE CHIP



1-7,47	DB0-DB7	These are the bidirectional Data Bus signals. They are for communication between the VIC and the processor, and can only be accessed during AEC high.
8	IRQ	Interrupt output. Generates a low interrupt signal.
9	LP	Light Pen. Edge triggered latch for light pen input.
10	BA	Bus Available output. Used to DMA the processor.
11	DMARQST	External DMA request input. Pulled high on the C128.
12	AEC	Address Enable Control output. Goes high for processor enable on the shared bus, low for VIC cycle and VIC or external DMA.
13	CS	Chip select input. A low signal selects the VIC chip.
14	R/W	Standard 8502 bus Read/Write for interface between the processor and the various VIC registers.
15	DMAACK	External DMA Acknowledge. Not used in the C128 design.
16	COLOR	Output containing all color based video information: chrominance, color reference burst, and color of display data.
17	SYNC	Output containing composite sync information, video data, and luminance information.
18	1MHz	The 1MHz system clock. All system bus activity is referenced to this clock.
19	RAS	Row Address Strobe output for DRAMS.
20	CAS	Column Address Strobe output for DRAMS.
21	MUX	Address Multiplexing control output for DRAMS.
22	I/O ACC	Input from the PLA, indicating an I/O chip access for clock stretching.
23	2MHz	This is the changing system clock, which will be either 1MHz or 2MHz. If the 2MHz bit is clear, no VIC or external DMA is taking place, and no I/O operation is occurring, the clock will be 2MHz. It will be 1MHz otherwise.
24	VSS	Ground.
25	Z80 PHI	The special 4MHz Z-80 clock.
26-28	K0-K2	Extended keyboard strobe bits.
29	PH CL	The Color Clock input, used to derive the chroma signal, 14.31818 MHZ NTSC.
30	PH IN	The fundamental shift rate clock input, also called the DOT clock. Used as the reference for all system clocks. Determines the dot transfer rate to the display.
31	A11	See A8-A11 below.
32-37	A0-A5	Multiplexed Address Lines. During row address time, A_0 - A_5 are driven on A_0 - A_5. During column address time, A_8 - A_{13} are driven on A_0 - A_5 and A_6 is held at one. During a processor write or read, A_0 - A_5 serve as address inputs which latch on the low edge of $\overline{RAS}$.
38, 39	A6, A7	Used as VIC address lines.
31, 40-42	A8-A11	Static Address lines. These address lines are used for non-multiplexed VIC memory accesses, such as to Character ROM and Color RAM.
43-46	DB8-DB11	These are the extended data bus signals. They are used for VIC communication with the Color RAM.
47	DB7	See Pins 1-7, 47, DB0-DB7.
48	VCC	5VDC input.